ABSTRACT

A pseudo-noise (PN) encoded digital data clock recovery circuit for recovering an original bit stream from a received chip stream includes a correlator, a phase controller, and a bit clock generator. The correlator correlates a pseudo-noise sequence with the received chip stream and generating a correlator output. The pseudo-noise sequence modulates the original bit stream. The phase controller is configured and arranged to histogram the correlator output of the correlator over the plurality of bit periods. The bit clock generator generates a bit clock which determines a sampling position of the received chip stream to recover the original bit stream from the received chip stream. The bit clock generator uses the histogram of the correlator output to select/adjust the sample position for the bit clock. Accordingly, the pseudo-noise encoded digital data clock recovery circuit reliably synchronizes the bit clock, identifies a correct bit alignment, and tracks a correct bit alignment over time, for example, more than two bit periods, etc.